

What is claimed is:

1. A semiconductor memory device, comprising:
a main amplifier for amplifying an output from a bit
5 line sensing amplifier and outputting the amplified output to
a first data line;
an input/output multiplexer connected to the first data
line;
a repeater connected to the first data line;
10 an input/output write unit for receiving a data to be
written and outputting the data to a second data line; and
a write driver connected to the second data line for
transferring the data on the second data line to the bit line
sensing amplifier.

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2. The semiconductor memory device as recited in claim 1,
wherein the input/output multiplexer includes:
a clocked inverter for receiving an output from the
first data line; and
20 a latch connected to an output terminal of the clocked
inverter, wherein there is no charge sharing between the latch
and the first data line.

3. The semiconductor memory device as recited in claim 2,
25 wherein the input/output multiplexer includes:
a control unit for receiving an address signal, a mode
signal and a write signal to control the clocked inverter;

a clocked inverter for receiving an output from the first data line; and

a latch connected to an output terminal of the clocked inverter, wherein the write signal is activated in a write 5 operation.

4. The semiconductor memory device as recited in claim 3, wherein the control unit includes:

a first inverter for receiving an address signal to 10 invert the address signal;

a first NAND gate for receiving a mode signal and an output from the first inverter;

a second NAND gate for receiving the mode signal and the address signal;

15 a second inverter for receiving the write signal to invert the write signal;

a third inverter for inverting an output from the second inverter;

a fourth inverter for inverting an output from the first 20 NAND gate;

a third NAND gate for receiving an output from the second inverter and an output from the third inverter; and

a fourth NAND gate for receiving an output from the second inverter and an output from the fourth inverter.

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5. The semiconductor memory device as recited in claim 1, wherein the input/output write unit includes:

a transferring gate for receiving a data and selectively outputs the data;

 an operating unit for transferring an output from the transferring gate to a second data line; and

5 a control unit for generating a control signal to control the transferring gate and the operating unit, wherein the input/output write unit is a static type having a clocked inverter.

10 6. The semiconductor memory device as recited in claim 5, wherein the control unit includes:

 a tenth inverter for receiving and inverting a data input strobe signal;

15 a eleventh inverter for inverting an output from the tenth inverter; and

 a twelfth inverter for receiving and inverting an even-odd signal.

7. The semiconductor memory device as recited in claim 6,
20 wherein the control unit includes:

 a first clocked inverter for receiving an output from the transferring gate to invert the output from the transferring gate;

25 a second clocked inverter and a thirteenth inverter for latching an output from the first clocked inverter;

 a third clocked inverter for receiving an output from the first clocked inverter to invert the output from the first

clocked inverter; and

a fourth clocked inverter and a fourteenth inverter for latching an output from the third clocked inverter.

5 8. The semiconductor memory device as recited in claim 1, further comprising a repeater connected to the second data line.

9. The semiconductor memory device as recited in claim 1,
10 wherein one of the first data line and the second data line is selected depending on a write operation or a read operation.